ABSTRACT

The multiple bit, vertical memory cell includes a vertical metal oxide semiconductor field effect transistor (MOSFET) extending horizontally outward from a substrate. The MOSFET has a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a gate insulator. The gate insulator may be a composite of oxide-nitride-aluminum oxide. The MOSFET is operated with either the first source/drain region or the second source/drain region serving as the source region, depending on the voltages applied to these regions. A negative substrate bias is applied during programming and erasing operations to enhance hot carrier injection.